

THAT WHICH IS CLAIMED IS:

1. Process for reducing the electrical consumption of a transmitter/receiver of digital information, in particular a cellular mobile telephone, comprising a frequency synthesizer stage controlled by

5 an automatic frequency control algorithm and able to deliver at least one reference signal of chosen frequency to the transmission/reception stage of the telephone and a master-clock signal of chosen frequency to the modulation/demodulation means of the

10 transmitter/receiver, characterized in that the reference signal or signals are generated with a predetermined transmission accuracy, on the basis of at least a first fractional-division phase-locked loop (EPLL) controlled by the automatic frequency control

15 algorithm and receiving a base signal (SBA) having a predetermined base frequency and a base accuracy lower than the said transmission accuracy, a clock signal (SH) is generated with a predetermined accuracy, on the basis of a second fractional-division phase-locked loop

20 (MCPLL) controlled by the automatic frequency control algorithm and receiving the base signal, and when the transmission/reception stage is inactive, the second fractional-division phase-locked loop (MCPLL) is rendered inactive, the base signal (SBA) then being the

25 master-clock signal, and when the transmission/reception stage is active, the second loop is activated, the clock signal (SH) delivered by this loop then being the master-clock signal (SHM).

2. Device for transmitting/receiving digital information, in particular cellular mobile telephone, comprising a transmission/reception stage (RXC, TXC), a

processing stage (DSP) connected to the transmission/
5 reception stage and comprising modulation/demodulation
means (MDM) and automatic frequency control means
(AFC), and a frequency synthesizer stage controlled by
the automatic frequency control means and able to
deliver at least one reference signal of chosen
10 frequency to the transmission/reception stage and a
master-clock signal of chosen frequency to the
modulation/demodulation means, characterized in that
the frequency synthesizer stage comprises
at least a first fractional-division phase-
15 locked loop (EPLL) whose output, linked to the
transmission/reception stage, is able to deliver, with
a predetermined transmission accuracy, the reference
signal and a second fractional-division phase-locked
loop (MCPLL) whose output is able to deliver, with a
20 predetermined accuracy, a clock signal (SH), each loop
being able to adopt on command an active state and an
inactive state and possessing a control input linked to
the automatic frequency control means, as well as an
input for receiving a base signal (SBA) emanating from
25 an oscillator (QT) and having a predetermined base
frequency and a base accuracy lower than the said
transmission accuracy, and
controllable switching means (MCM) possessing
a first state linking the output of the oscillator (QT)
30 to the modulation/demodulation means (MDM) and a second
state linking the output of the second loop (MCPLL) to
the modulation/demodulation means,
and in that it furthermore comprises control
means (MCD) able to place the second loop in its
35 inactive state and the switching means in their first

state, and to place the second loop in its active state and the switching means in their second state.

3. Device according to claim 1, characterized in that each loop (EPLL, MCPLL) is a delta-sigma modulation fractional-division phase-locked loop.

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